What is claimed is:

1. A predistorter configured for use with an RF power amplifier, the predistorter comprising:

a vector modulator configured to receive an RF input signal and apply a correction thereto using correction factors;

a data structure coupled to the vector modulator and storing the correction factors;

the correction factors of the data structure compensating for amplitude and phase non-linearities in the responses of both the RF power amplifier and the vector modulator.

2. The predistorter of claim 1, the data structure comprising a first pair of look-up tables, one for in-phase (I) and one for quadrature-phase (Q) signal components, configured for storing amplitude and phase correction factors for the RF power amplifier and the vector modulator.

3. The predistorter of claim 2, the data structure further comprising a second pair of look-up tables, one for in-phase (I) and one for quadrature-phase (Q) signal components, configured for storing correction factors to compensate for memory effects in the response of the RF power amplifier.

4. The predistorter of claim 3, further comprising a differentiator circuit coupled to at least one of each of the first and second pairs of look-up tables and configured to apply a difference equation to the correction factors in compensating for memory effects in the RF power amplifier.

5. The predistorter of claim 4, the differentiator circuit comprising:

a subtracter coupled to the first pair and second pairs of look-up tables and configured to subtract a previous correction factor from the second pair of look-up tables from a current correction factor from the first pair of look-up tables;

a first delay circuit coupled intermediate the second pair of look-up tables and the subtracter and configured to delay correction factors from the second pair of look-up tables;

a second delay circuit coupled to the subtracter and configured to delay the difference between the current and the previous correction factors; and

a summer coupled to the second delay circuit and the second pair of look-up tables and configured to add the difference between the current and previous correction factors to a subsequent correction factor to arrive at a correction factor that is used to compensate for memory effects in an RF power amplifier.

6. The predistorter of claim 4, further comprising a coupler coupled to the vector modulator and the look-up tables and configured to receive the RF input signal and sample a portion of the RF input signal and select correction factors from the look-up tables based on the sampled portion of the RF input signal;

wherein the predistorter modifies the RF input signal as a function of both instantaneous input signal envelope and the rate of change in the input signal envelope.

7. The predistorter of claim 6, further comprising an envelope detector disposed intermediate the coupler and the look-up tables and configured to generate an analog signal that is representative of the instantaneous input signal envelope from the sampled portion of the RF input signal.

8. The predistorter of claim 7, further comprising an analog-to-digital converter disposed intermediate the envelope detector and the look-up tables and configured to convert the analog signal to a digital signal.

9. The predistorter of claim 3, further comprising a circuit configured to transfer correction factors into the data structure.

10. The predistorter of claim 3, the circuit further configured to transfer scaling factors into the data structure, the data structure configured to calculate correction factors for storage in the second pair of look-up tables from the scaling factors based on a polynomial.

11. The predistorter of claim 10, wherein the polynomial is of the form $Wx^2 + Yx^4$, and W and Y are scaling factors.

12. The predistorter of claim 10, wherein the data structure is further configured to scale the calculated correction factors.

13. The predistorter of claim 10, the first circuit comprising:

a serial data link configured to receive and transmit at least one of correction and scaling factors;

a dual-port buffer coupled to the serial data link and the data structure; and,

a transfer controller coupled to the serial data link, the dual-port buffer, and the data structure and configured to control the transfer of at least one of correction and scaling factors.

14. The predistorter of claim 10, the second circuit comprising:

a first multiplier configured to receive a first scale factor associated with the second pair of look-up tables;

a second multiplier configured to receive a second scale factor associated with the second pair of look-up tables;

a counter coupled to the data structure and configured to provide a count and address the second set of look-up tables comprising the data structure based on the count;

a third multiplier coupled to the counter and the first multiplier and configured to square the count;

a fourth multiplier coupled to the second and third multipliers and configured to square the squared count, raising the count to the fourth power;

wherein the squared count and the count to the fourth power are combined with first and second multipliers to calculate corrections factors.

15. An amplifier system, the system comprising:

an RF power amplifier; and

a predistorter coupled to the RF power amplifier, the predistorter comprising:

a vector modulator configured to receive an RF input signal and apply a correction thereto using correction factors;

a data structure coupled to the vector modulator and storing the correction factors;

the correction factors of the data structure compensating for amplitude and phase non-linearities in the response of both the RF power amplifier and the modulator.

16. The amplifier system of claim 15, the data structure comprising a first pair of look-up tables, one for in-phase (I) and one for quadrature-phase (Q) signal components, configured for storing amplitude and phase correction factors for the RF power amplifier and the vector modulator.

17. The amplifier system of claim 16, the data structure further comprising a second pair of look-up tables, one for in-phase (I) and one for quadrature-phase (Q) signal components, configured for storing correction factors to compensate for memory effects in the response of the RF power amplifier.

18. The amplifier system of claim 17, the predistorter further comprising a differentiator circuit coupled to at least one of each of the first and second pairs of look-up tables and configured to apply a difference equation to the correction factors in compensating for memory effects in the RF power amplifier.

19. The amplifier system of claim 18, the differentiator circuit comprising:

a subtracter coupled to the first pair and second pairs of look-up tables and configured to subtract a previous correction factor from the second pair of look-up tables from a current correction factor from the first pair of look-up tables;

a first delay circuit coupled intermediate the second pair of look-up tables and the subtracter and configured to delay correction factors from the second pair of look-up tables;

a second delay circuit coupled to the subtracter and configured to delay the difference between the current and the previous correction factors; and

a summer coupled to the second delay circuit and the second pair of look-up tables and configured to add the difference between the current and the previous correction factors to a subsequent correction factor to arrive at a correction factor that is used to compensate for memory effects in the RF power amplifier.

20. The amplifier system of claim 18, the predistorter further comprising a coupler coupled to the vector modulator and the look-up tables and configured to receive the RF input signal and sample a portion of the RF input signal and select correction factors from the look-up tables based on the sampled portion of the RF input signal;

wherein the predistorter modifies the RF input signal as a function of both instantaneous input signal envelope and the rate of change in the input signal envelope.

21. The amplifier system of claim 20, the predistorter further comprising an envelope detector disposed intermediate the coupler and the look-up tables and configured to generate an analog signal that is representative of the instantaneous input signal envelope from the sampled portion of the RF input signal.

22. The amplifier system of claim 21, the predistorter further comprising an analog-to-digital converter disposed intermediate the envelope detector and the look-up tables and configured to convert the analog signal to a digital signal.

23. The amplifier system of claim 17, the predistorter further comprising a circuit configured to transfer correction factors into the data structure.

24. The amplifier system of claim 23, the circuit further configured to transfer scaling factors into the data structure, the data structure configured to calculate correction factors for storage in the second pair of look-up tables from the scaling factors based on a polynomial.

25. The amplifier system of claim 24, wherein the polynomial is of the form $Wx^2 + Yx^4$, and W and Y are scaling factors.

26. The amplifier system of claim 24, wherein the data structure is further configured to scale the calculated correction factors.

27. The amplifier system of claim 24, the first circuit comprising:

a serial data link configured to receive and transmit at least one of correction and scaling factors;

a dual-port buffer coupled to the serial data link and the data structure; and,

a transfer controller coupled to the serial data link, the dual-port buffer, and the data structure and configured to control the transfer of at least one of correction and scaling factors.

28. The amplifier system of claim 24, the second circuit comprising:

a first multiplier configured to receive a first scale factor associated with the second pair of look-up tables;

a second multiplier configured to receive a second scale factor associated with the second pair of look-up tables;

a counter coupled to the data structure and configured to provide a count and address the second set of look-up tables comprising the data structure based on the count;

a third multiplier coupled to the counter and the first multiplier and configured to square the count;

a fourth multiplier coupled to the second and third multipliers and configured to square the squared count, raising the count to the fourth power;

wherein the squared count and the count raised to the fourth power are combined with the first and second multipliers to calculate corrections factors.

29. A circuit for use in a predistorter having first and second pairs of look-up tables, the circuit comprising:

a subtracter coupled to the first and second pairs of look-up tables and configured to subtract a previous correction factor from the second pair of look-up tables from a current correction factor from the first pair of look-up tables;

a first delay circuit coupled intermediate the second pair of look-up tables and the subtracter and configured to delay correction factors from the second pair of look up tables;

a second delay circuit coupled to the subtracter and configured to delay the difference between the current and previous correction factors; and

a summer coupled to the second delay circuit and the second pair of look-up tables and configured to add the difference between the current and previous correction factors to a subsequent correction factor to arrive at a correction factor that is used to compensate for memory effects in an RF power amplifier.

30. A data structure for use with an RF power amplifier comprising:

look-up tables for storing correction factors that correct for memory effects in the RF power amplifier;

the data structure configured to use a polynomial to calculate the correction factors and populate the look-up tables.

31. The data structure of claim 30, the data structure configured to receive scaling factors and applying the scaling factors to the polynomial to calculate the correction factors.

32. The data structure of claim 31, the data structure further configured to receive an offset and offset the polynomial to reduce the memory size required by the look-up tables.

33. The data structure of claim 31 further comprising a counter configured to address the look-up tables based on a count.

34. The data structure of claim 31 further comprising a transfer controller coupled to the counter and configured to initiate counting.

35. The data structure of claim 31 further comprising:

a switch configured to selected between two scaling factors; and,

a transfer controller configured to control the switch.

36. The data structure of claim 31, further comprising:

a counter configured to provide a count; and,

a multiplier coupled to the counter and configured to square the count.

37. The data structure of claim 36 further comprising a second multiplier coupled to the first multiplier and configured to multiply a scale factor by the squared count.

38. The data structure of claim 37 further comprising a summer coupled to the second multiplier and configured to add an offset to the product of the scale factor and the squared count.

39. The data structure of claim 37 further comprising a second multiplier coupled to the first multiplier and configured to square the squared count.

40. The data structure of claim 39 further comprising a third multiplier coupled to the second multiplier and configured to multiply a scale factor by the count to the fourth power.

41. The data structure of claim 39 further comprising a summer coupled to the third multiplier and configured to add an offset to the product of a scale factor and the count to the fourth power.

42. A method of calibrating an amplifier system, the method comprising:

loading correction factors that correct for amplitude and phase non-linearities in the response of both an RF power amplifier and a modulator into a data structure.

43. The method of claim 42, further comprising:

transferring a scaling factor into the data structure; and,

calculating correction factors that correct for memory effects in the response of an RF power amplifier from the scaling factor in the data structure.

44. The method of claim 43, wherein the calculation is based on a polynomial.

45. The method of claim 44, wherein the polynomial is of the form $Wx^2 + Yx^4$, and W and Y are scaling factors.

46. The method of claim 43, wherein the polynomial is scaled.

47. A method of predistorting a signal applied to an RF power amplifier, the method comprising:

storing correction factors that correct for non-linearities in the response of both an RF power amplifier and a vector modulator in a data structure;

receiving an RF input signal using the vector modulator;

sampling a portion of the RF input signal power;

selecting correction factors from the data structure based on a portion of the RF input signal; and

applying the correction factors to the RF input signal using the vector modulator.

48. The method of claim 47, wherein the correction factors correct for non-linearities in the response of the RF power amplifier and the vector modulator are stored in a first pair of look-up tables.

49. The method of claim 47, further comprising:

transferring scaling factors into the data structure;

calculating correction factors that correct for memory effects in the response of the RF power amplifier; and

storing the correction factors that correct for memory effects in the response of the RF power amplifier in a second pair of look-up tables.

50. The method of claim 49, further comprising applying the difference equation to the correction factors so that the predistorted signal corrects for both amplitude and phase non-linearities in the RF power amplifier and the modulator and memory effects in the RF power amplifier.

51. The method of claim 49, where the calculation is based on a polynomial.

52. The method of claim 51, wherein the polynomial is of the form $Wx^2 + Yx^4$, and W and Y are scaling factors.

53. The method of claim 49, wherein the calculation scales the polynomial.